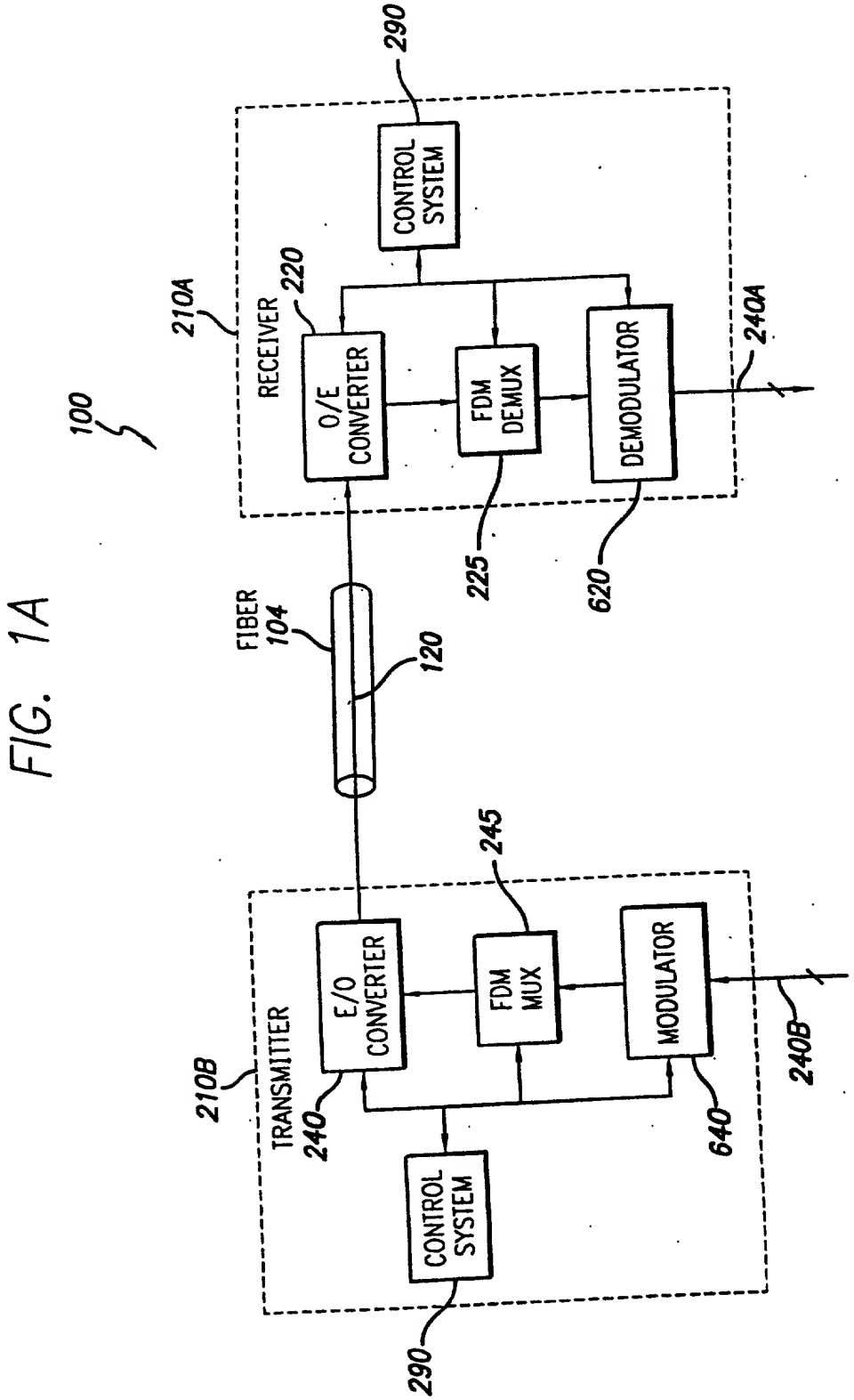

100
290
CONTROL SYSTEM
210A
RECEIVER
220
O/E CONVERTER
FDM DEMUX
DEMODULATOR
240A
225
620
FIBER
104
120
245
E/O CONVERTER
FDM MUX
MODULATOR
240B
210B
TRANSMITTER
240
640
CONTROL SYSTEM
290

FIG. 1A

FIG. 1B

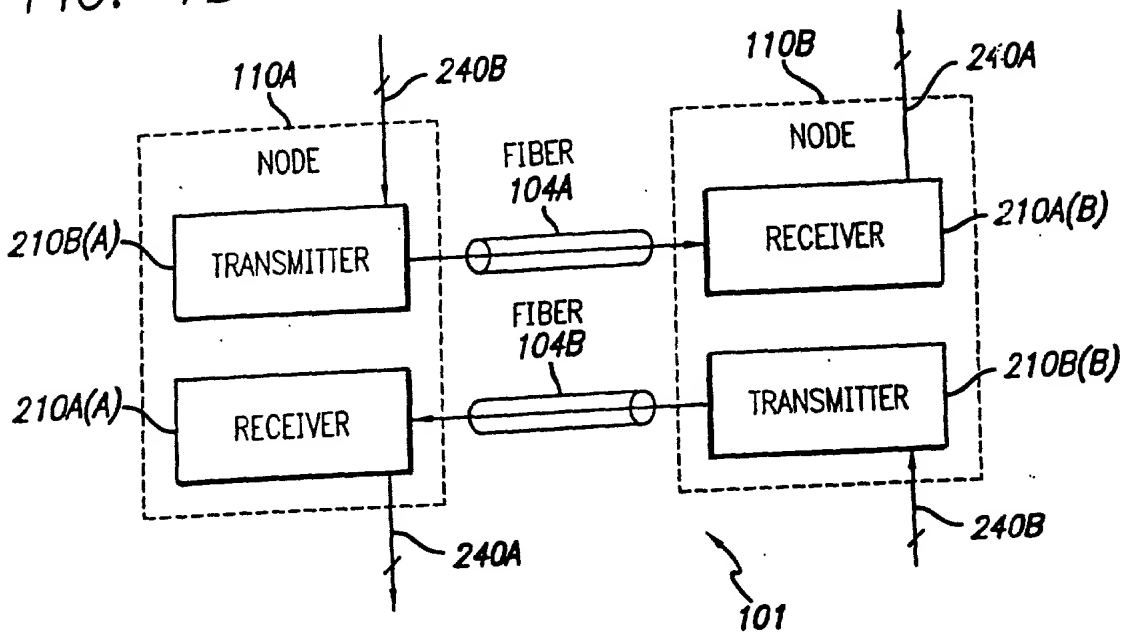

110A
240B
NODE
FIBER
104A
210B(A)
TRANSMITTER
RECEIVER
210A(B)
110B
240A
NODE
FIBER
104B
210A(A)
RECEIVER
TRANSMITTER
210B(B)
240A
240B
101

FIG. 2

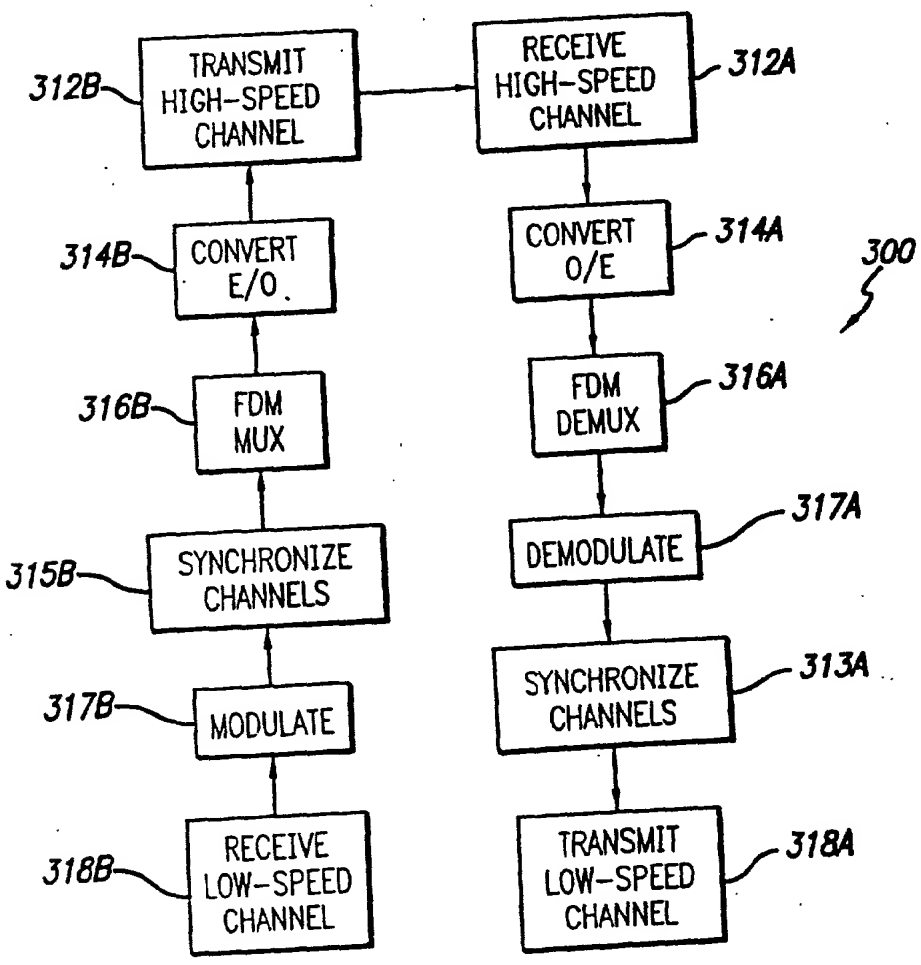

312B
TRANSMIT HIGH-SPEED CHANNEL
RECEIVE HIGH-SPEED CHANNEL
312A
314B
CONVERT E/O
CONVERT O/E
314A
300
316B
FDM MUX
FDM DEMUX
316A
315B
SYNCHRONIZE CHANNELS
DEMODULATE
317A
317B
MODULATE
SYNCHRONIZE CHANNELS
313A
318B
RECEIVE LOW-SPEED CHANNEL
TRANSMIT LOW-SPEED CHANNEL
318A

FIG. 3A

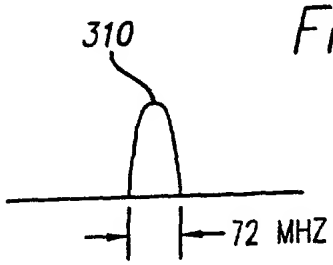


FIG. 3B

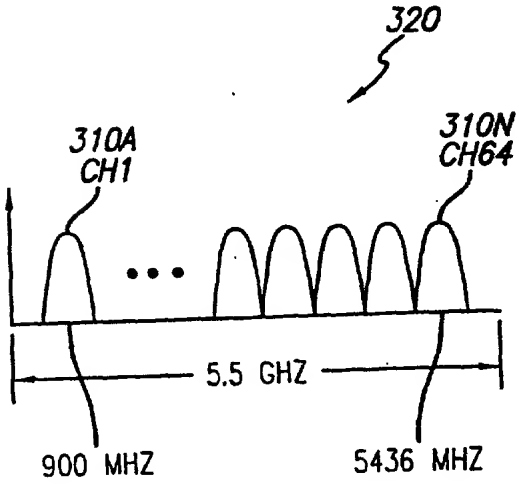
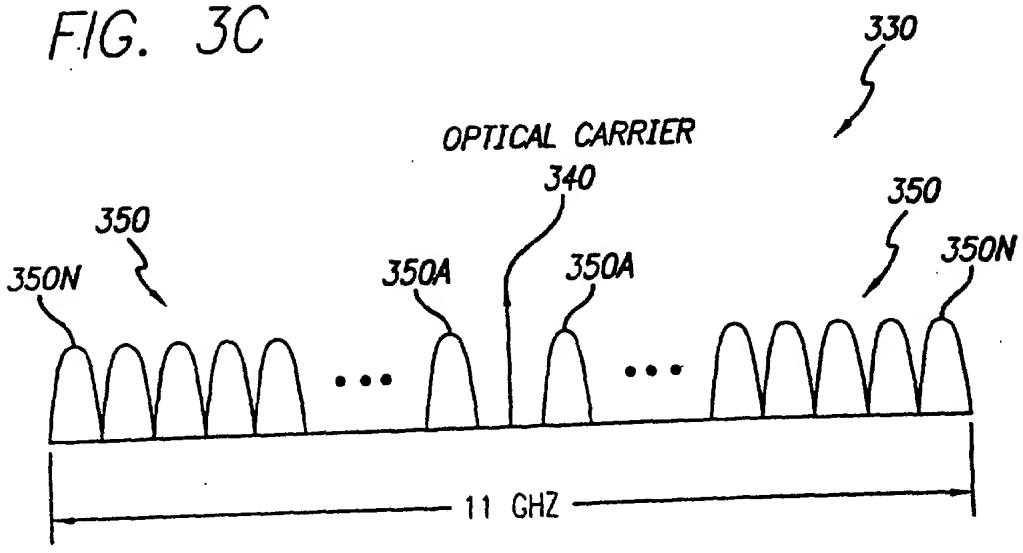


FIG. 3C



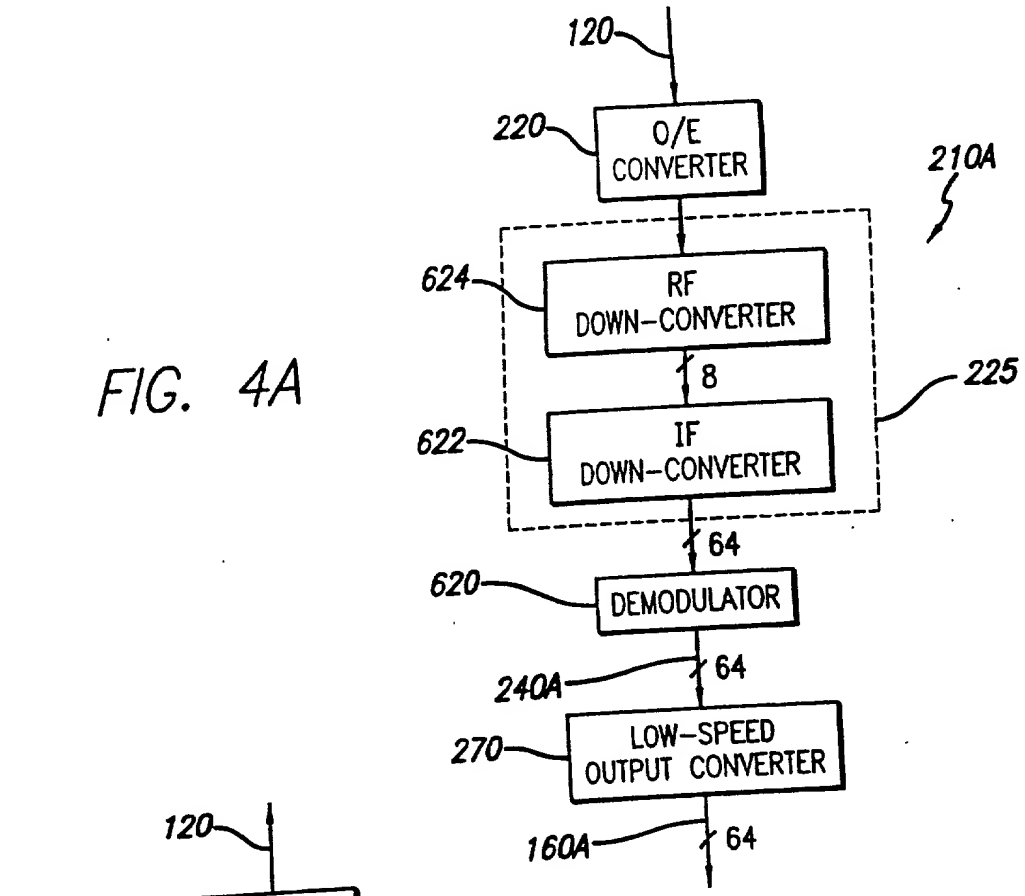

120
220
O/E CONVERTER
210A
624
RF DOWN-CONVERTER
8
225
622
IF DOWN-CONVERTER
64
620
DEMODULATOR
240A
64
270
LOW-SPEED OUTPUT CONVERTER
160A
64

FIG. 4A

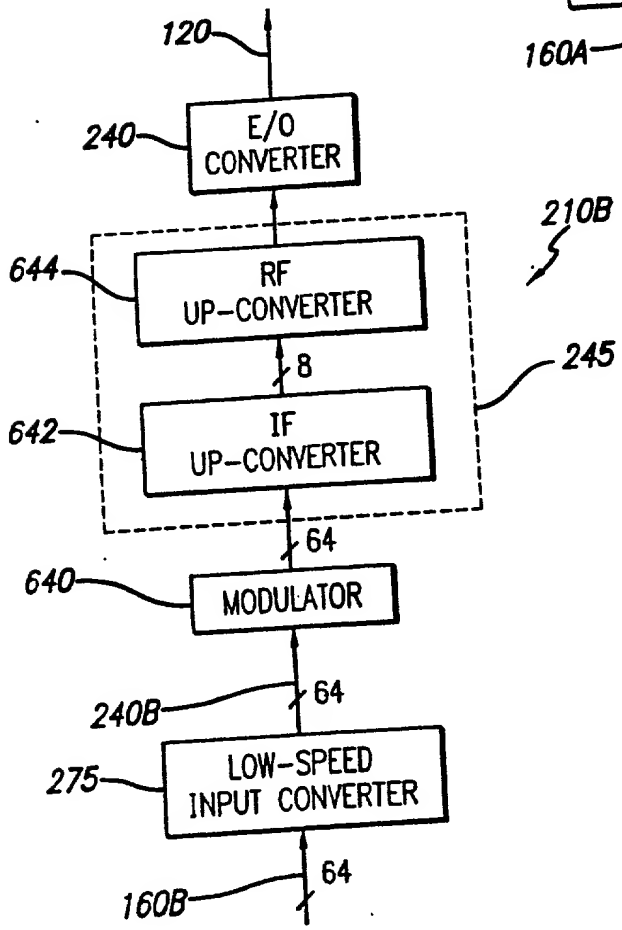

120
240
E/O CONVERTER
210B
644
RF UP-CONVERTER
8
245
642
IF UP-CONVERTER
64
640
MODULATOR
240B
64
275
LOW-SPEED INPUT CONVERTER
160B
64

FIG. 4B

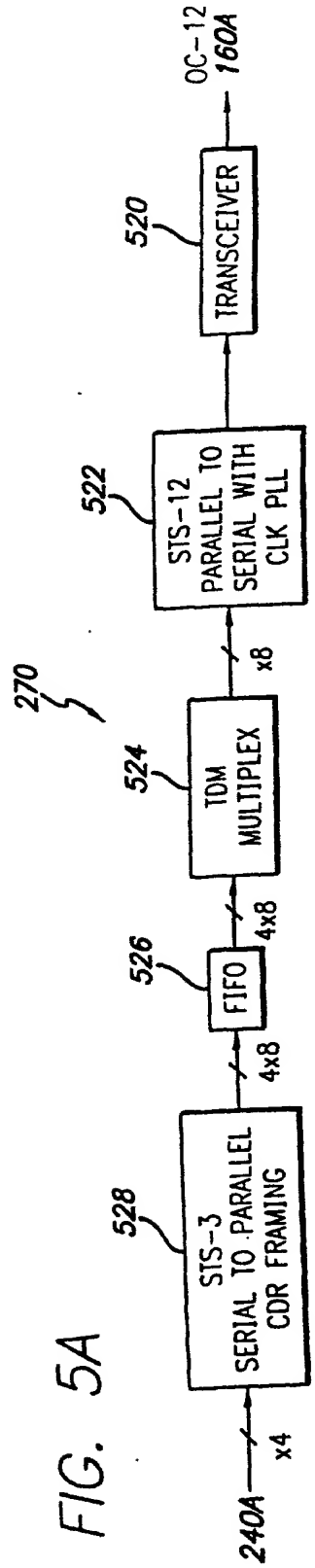

240A
x4
528
STS-3
SERIAL TO PARALLEL
CDR FRAMING
4x8
526
FIFO
4x8
524
TDM
MULTIPLEX
x8
270
522
STS-12
PARALLEL TO
SERIAL WITH
CLK PLL
520
TRANSCEIVER
OC-12
160A

FIG. 5A

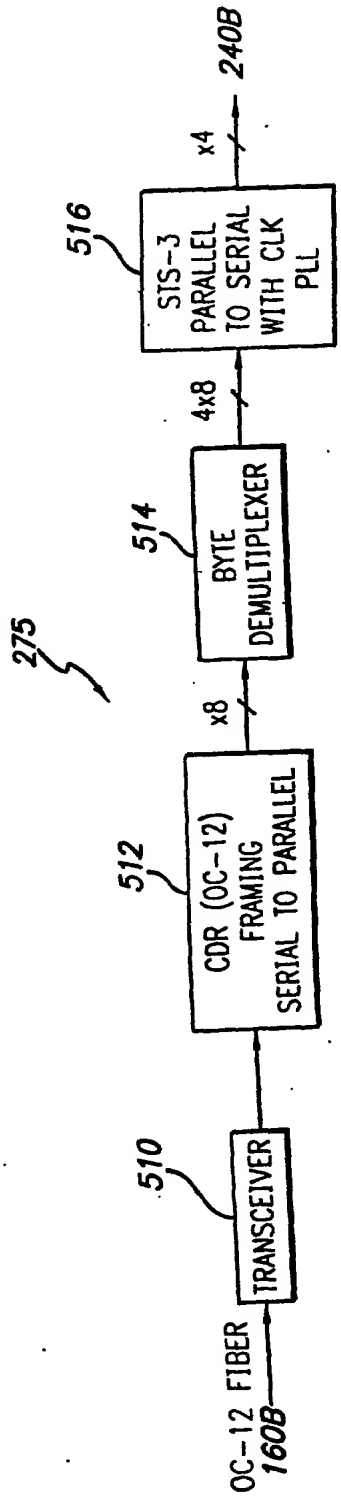

OC-12 FIBER
160B
510
TRANSCEIVER
512
CDR (OC-12)
FRAMING
SERIAL TO PARALLEL
x8
275
514
BYTE
DEMULTIPLEXER
4x8
516
STS-3
PARALLEL
TO SERIAL
WITH CLK
PLL
x4
240B

FIG. 5B

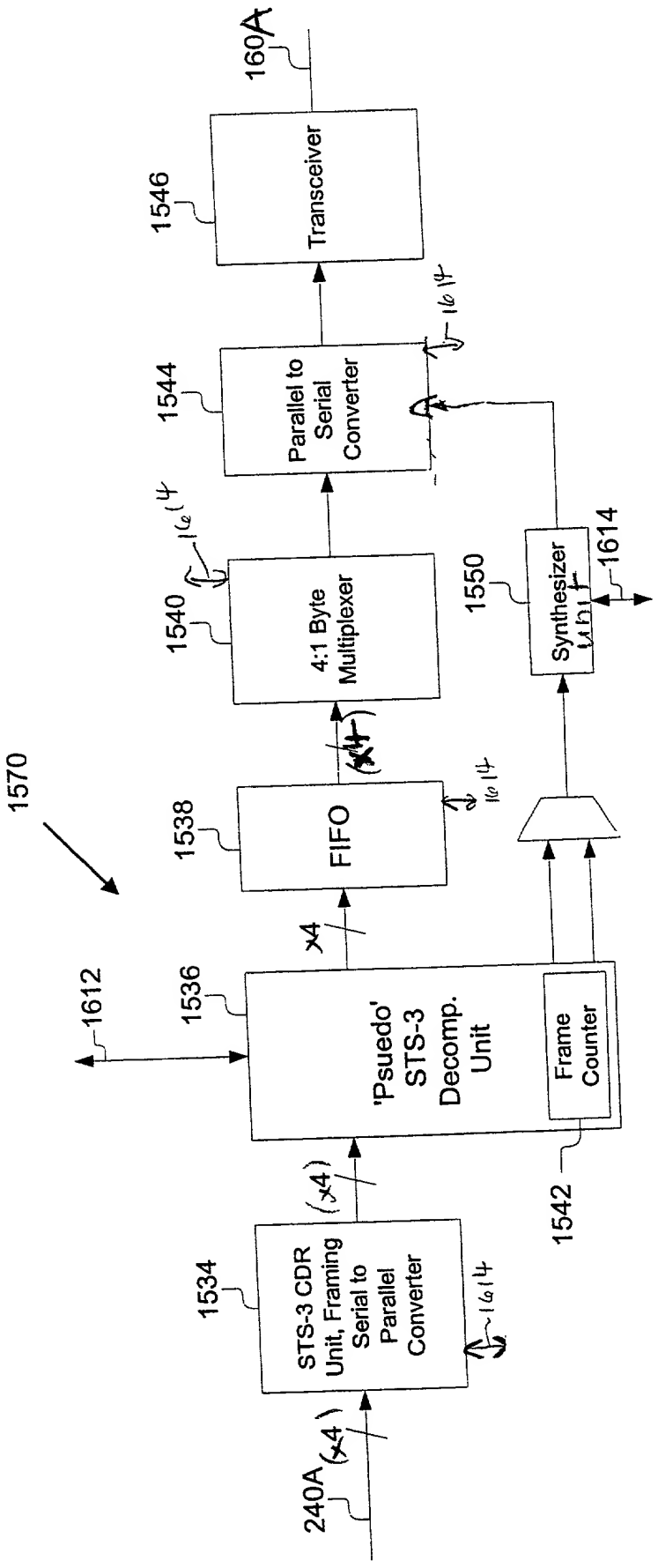

240A
(x4)
1534
STS-3 CDR Unit, Framing Serial to Parallel Converter
1614
(x4)
1536
'Psuedo' STS-3 Decomp. Unit
Frame Counter
1542
1612
1570
x4
1538
FIFO
1614
1540
4:1 Byte Multiplexer
1544
Parallel to Serial Converter
1614
1546
Transceiver
160A
1550
Synthesizer
1614

Figure 5C

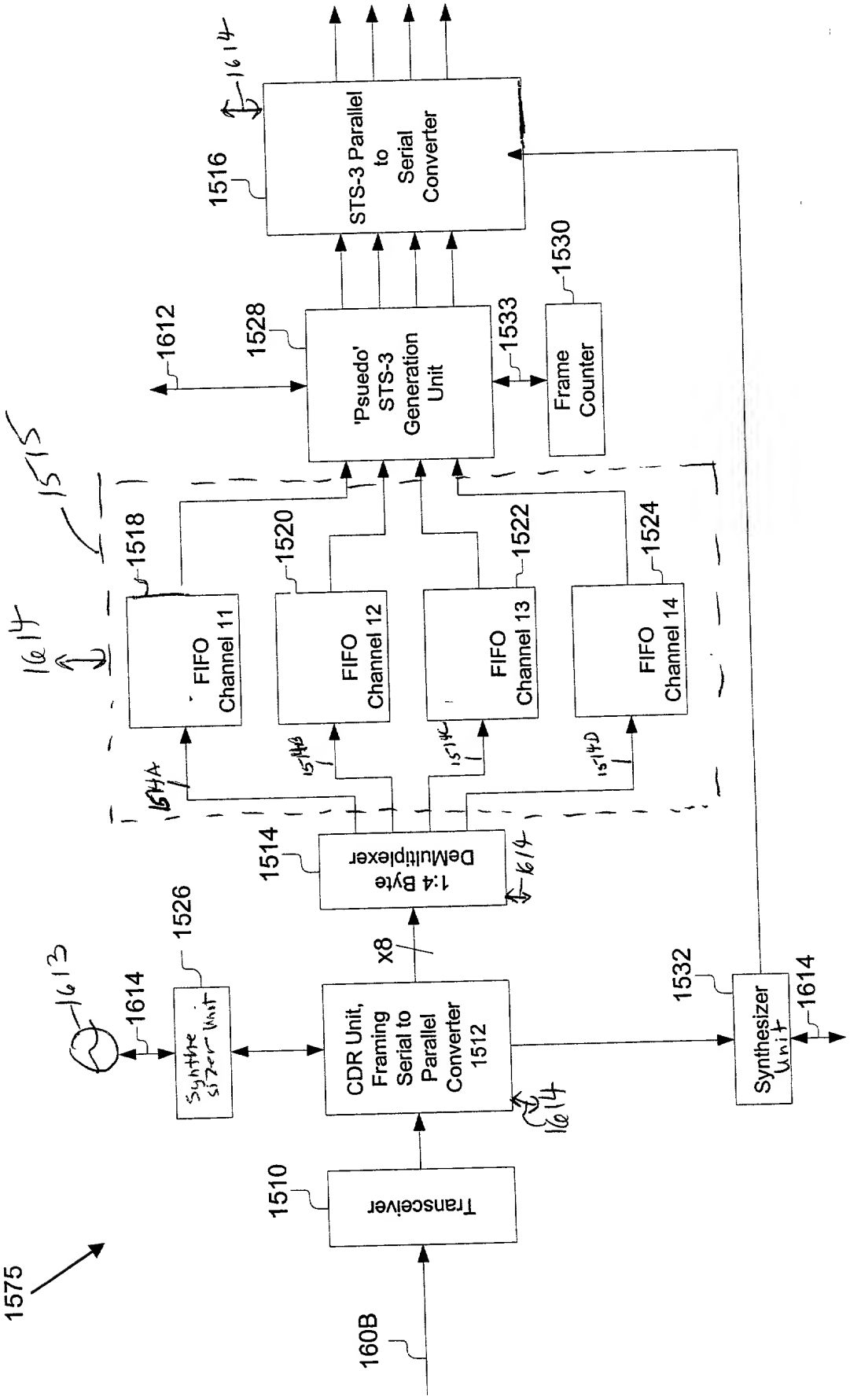

1575
160B
Transceiver
1510
CDR Unit, Framing Serial to Parallel Converter 1512
x8
1:4 Byte DeMultiplexer
1514
FIFO Channel 11
FIFO Channel 12
FIFO Channel 13
FIFO Channel 14
1518
1520
1522
1524
1515
'Psuedo' STS-3 Generation Unit
1528
Frame Counter
1530
1533
1612
STS-3 Parallel to Serial Converter
1516
1614
Synthesizer Unit
1532
1526
1613

Figure 5D

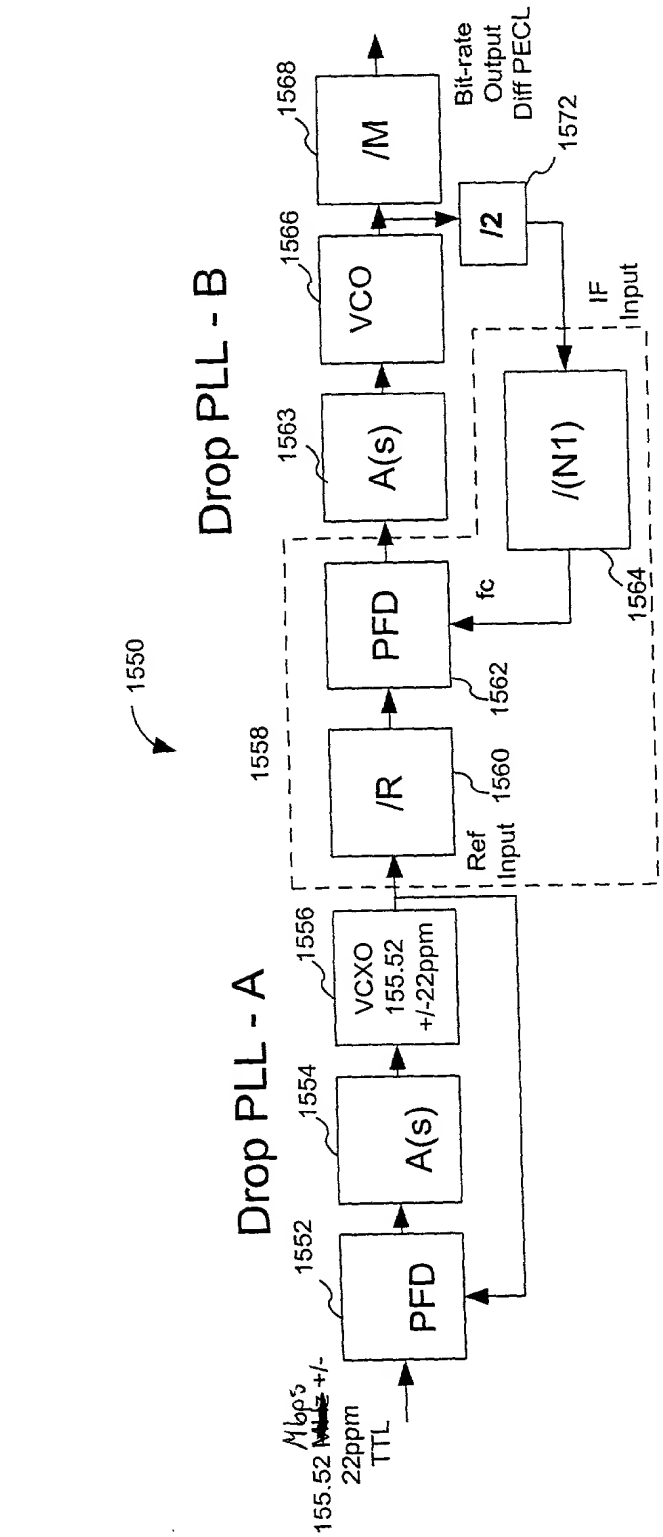

1550
Drop PLL - A
Drop PLL - B
1552
PFD
1554
A(s)
1556
VCXO
155.52
+/-22ppm
155.52 Mbps +/-
22ppm
TTL
1558
/R
1560
Ref
Input
1562
PFD
fc
1563
A(s)
1564
/(N1)
IF
Input
1566
VCO
1568
/M
Bit-rate
Output
Diff PECL
1572
/2

FIG. 5E

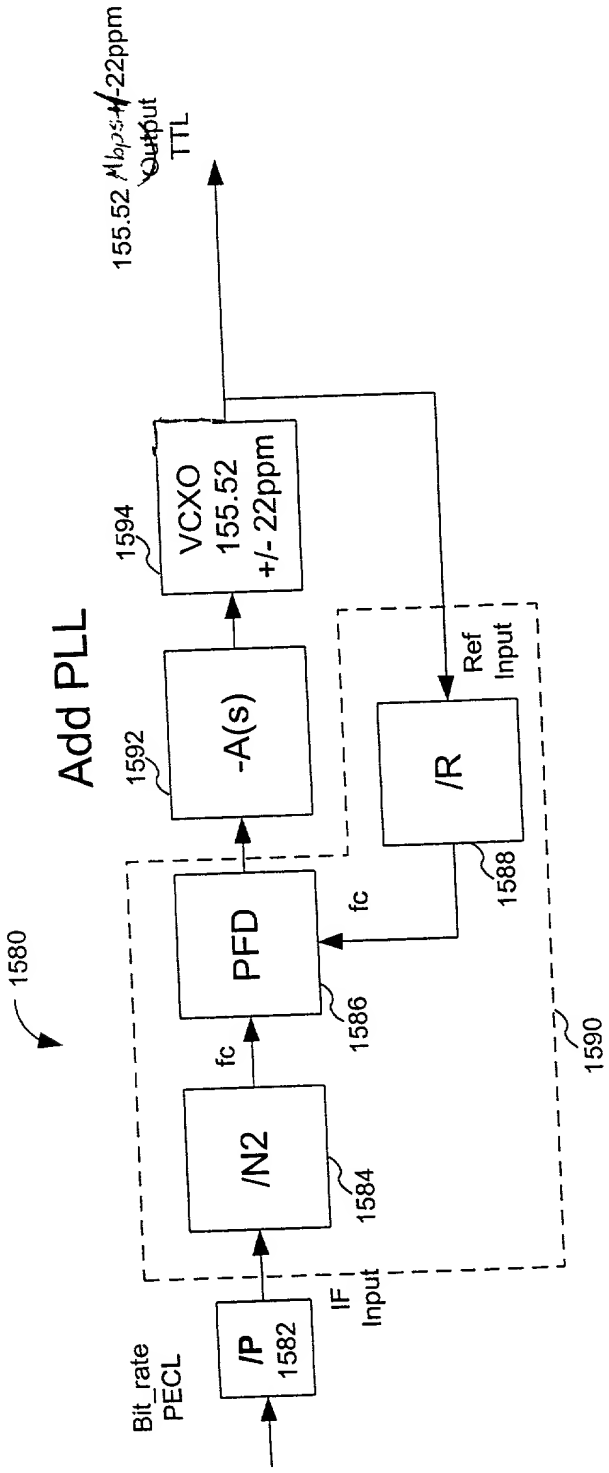

155.52 Mbps +/-22ppm
Output
TTL
Add PLL
1594
VCXO
155.52
+/- 22ppm
1592
-A(s)
Ref
Input
/R
1588
fc
PFD
1586
fc
/N2
1584
/P
1582
Bit_rate
PECL
IF
Input
1590
1580

FIG. 5F

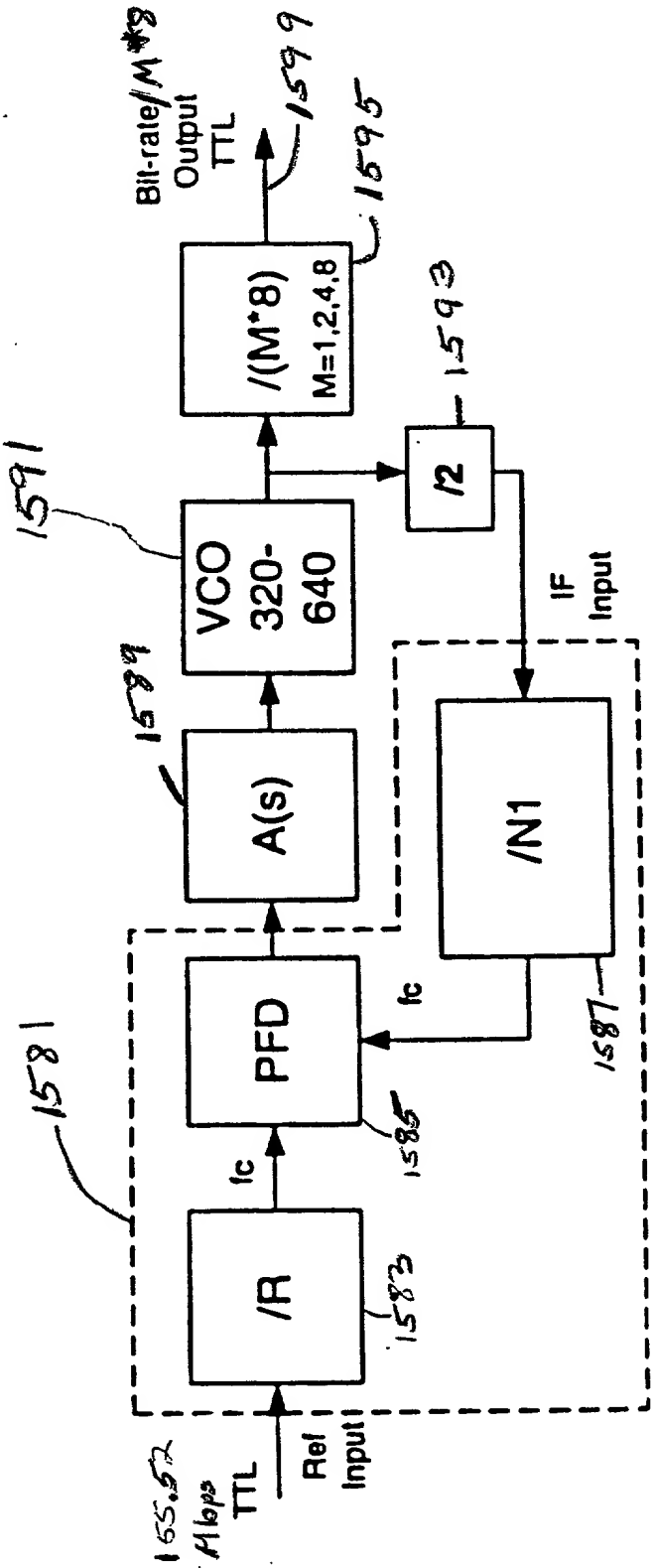

155.52 Mbps TTL
Ref Input
/R
1583
Ic
PFD
1585
Ic
1587
/N1
IF Input
1581
A(s)
1589
VCO 320-640
1591
/2
1593
/(M*8) M=1,2,4,8
1595
Bit-rate/M*8 Output TTL
1599

FIG. 5G

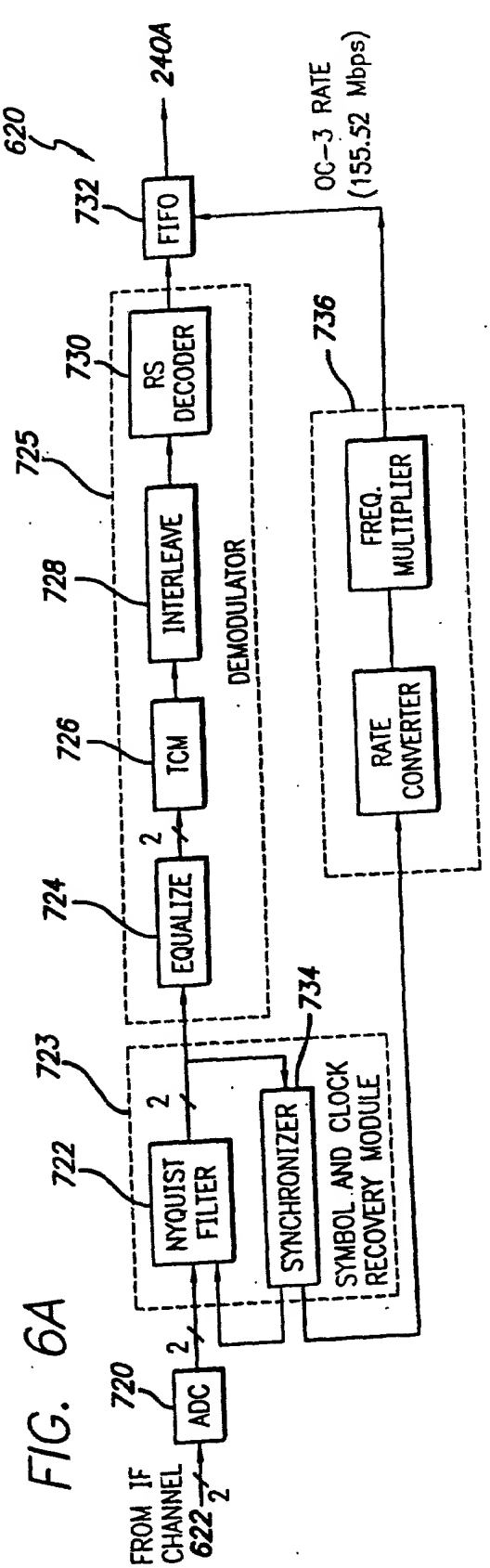

620
240A
732
FIFO
730
RS DECODER
725
728
INTERLEAVE
726
TCM
724
EQUALIZE
DEMODULATOR
736
FREQ. MULTIPLIER
RATE CONVERTER
OC-3 RATE (155.52 Mbps)
723
734
722
NYQUIST FILTER
SYNCHRONIZER
SYMBOL AND CLOCK RECOVERY MODULE
720
ADC
FROM IF CHANNEL
622
2

FIG. 6A

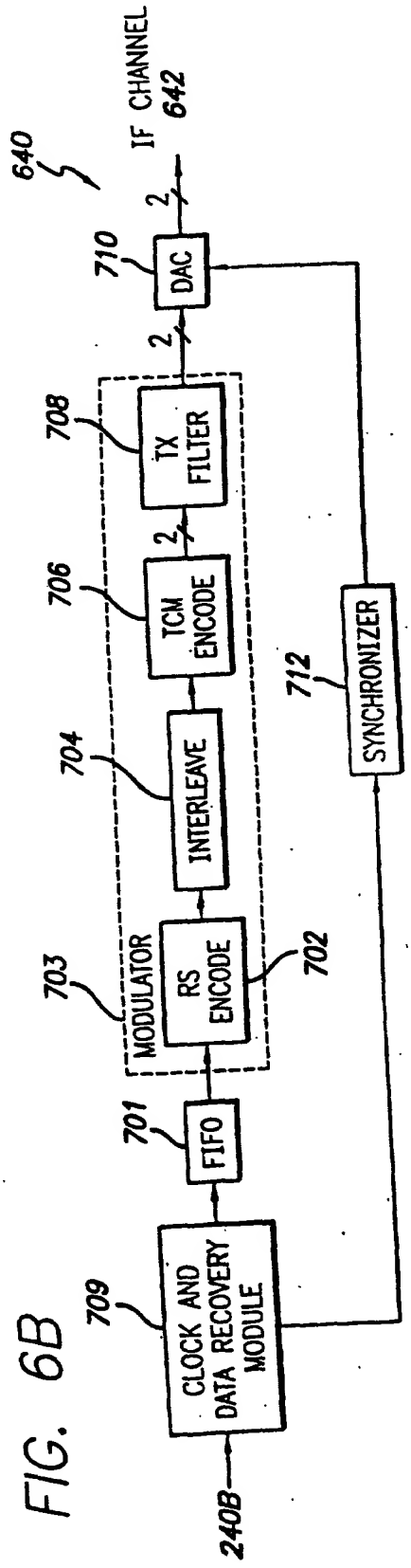

640
IF CHANNEL
642
2
710
DAC
708
TX FILTER
706
TCM ENCODE
704
INTERLEAVE
712
SYNCHRONIZER
703
MODULATOR
RS ENCODE
702
701
FIFO
709
CLOCK AND DATA RECOVERY MODULE
240B

FIG. 6B

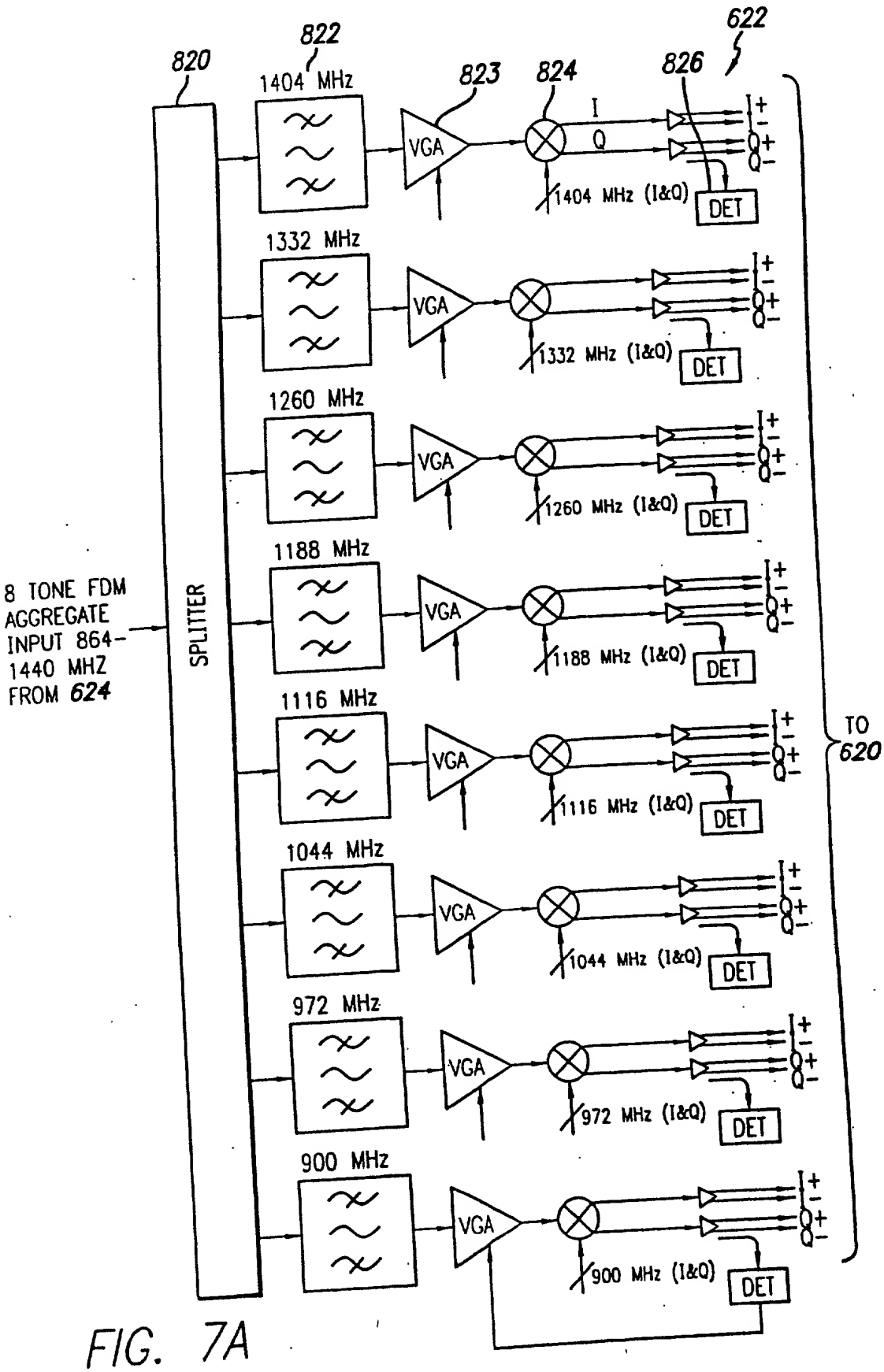

820
822
622
1404 MHz
823
824
826
VGA
I
Q
1404 MHz (I&Q)
DET
1332 MHz
1332 MHz (I&Q)
1260 MHz
1260 MHz (I&Q)
1188 MHz
1188 MHz (I&Q)
1116 MHz
1116 MHz (I&Q)
1044 MHz
1044 MHz (I&Q)
972 MHz
972 MHz (I&Q)
900 MHz
900 MHz (I&Q)
8 TONE FDM AGGREGATE INPUT 864-1440 MHZ FROM 624
SPLITTER
TO 620

FIG. 7A

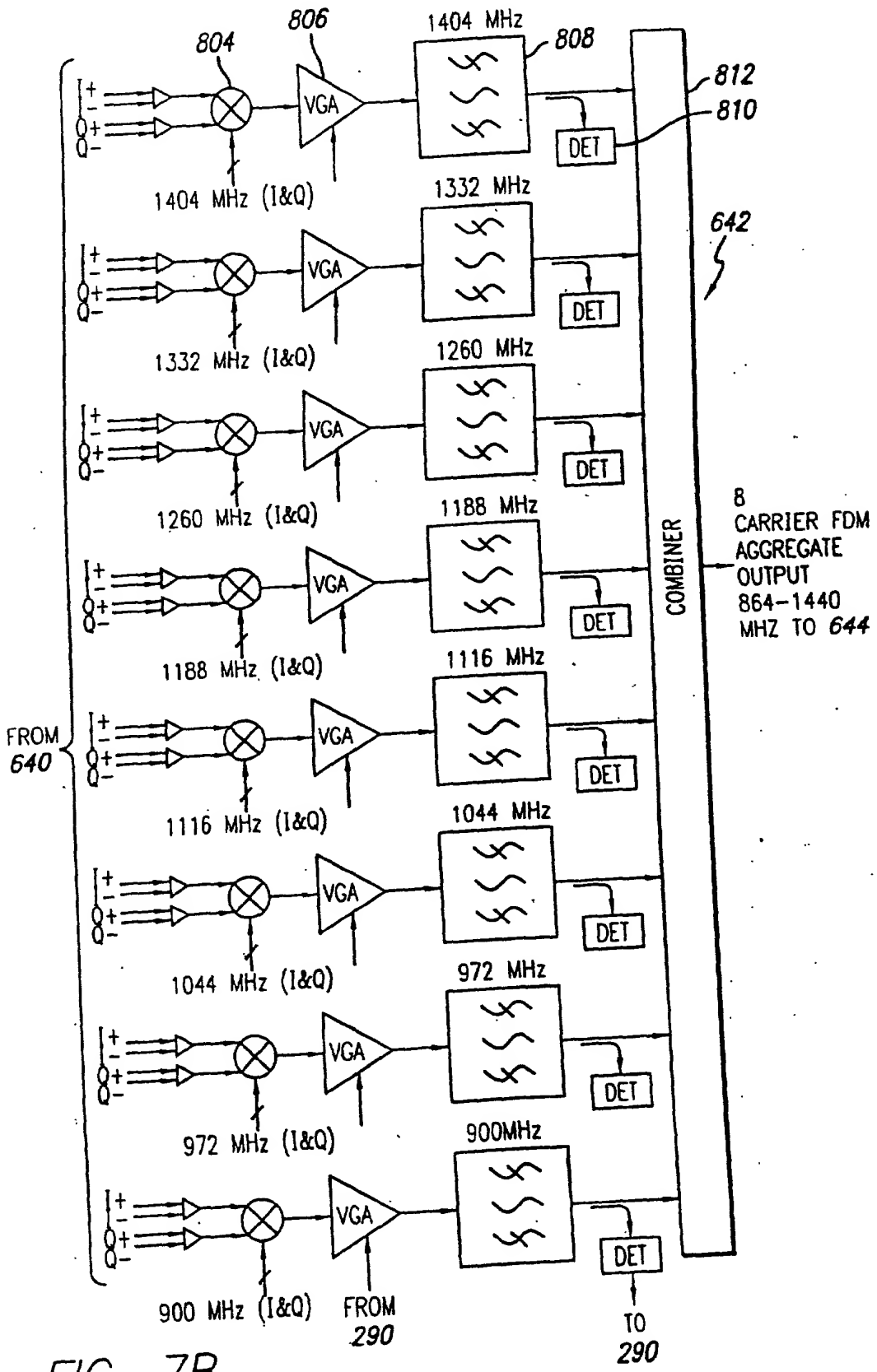

804
806
1404 MHz
808
812
810
642
VGA
DET
1404 MHz (I&Q)
1332 MHz
1332 MHz (I&Q)
1260 MHz
1260 MHz (I&Q)
1188 MHz
1188 MHz (I&Q)
1116 MHz
1116 MHz (I&Q)
1044 MHz
1044 MHz (I&Q)
972 MHz
972 MHz (I&Q)
900MHz
900 MHz (I&Q)
FROM 290
TO 290
FROM 640
COMBINER
8 CARRIER FDM AGGREGATE OUTPUT 864-1440 MHZ TO 644

FIG. 7B

FIG. 8A

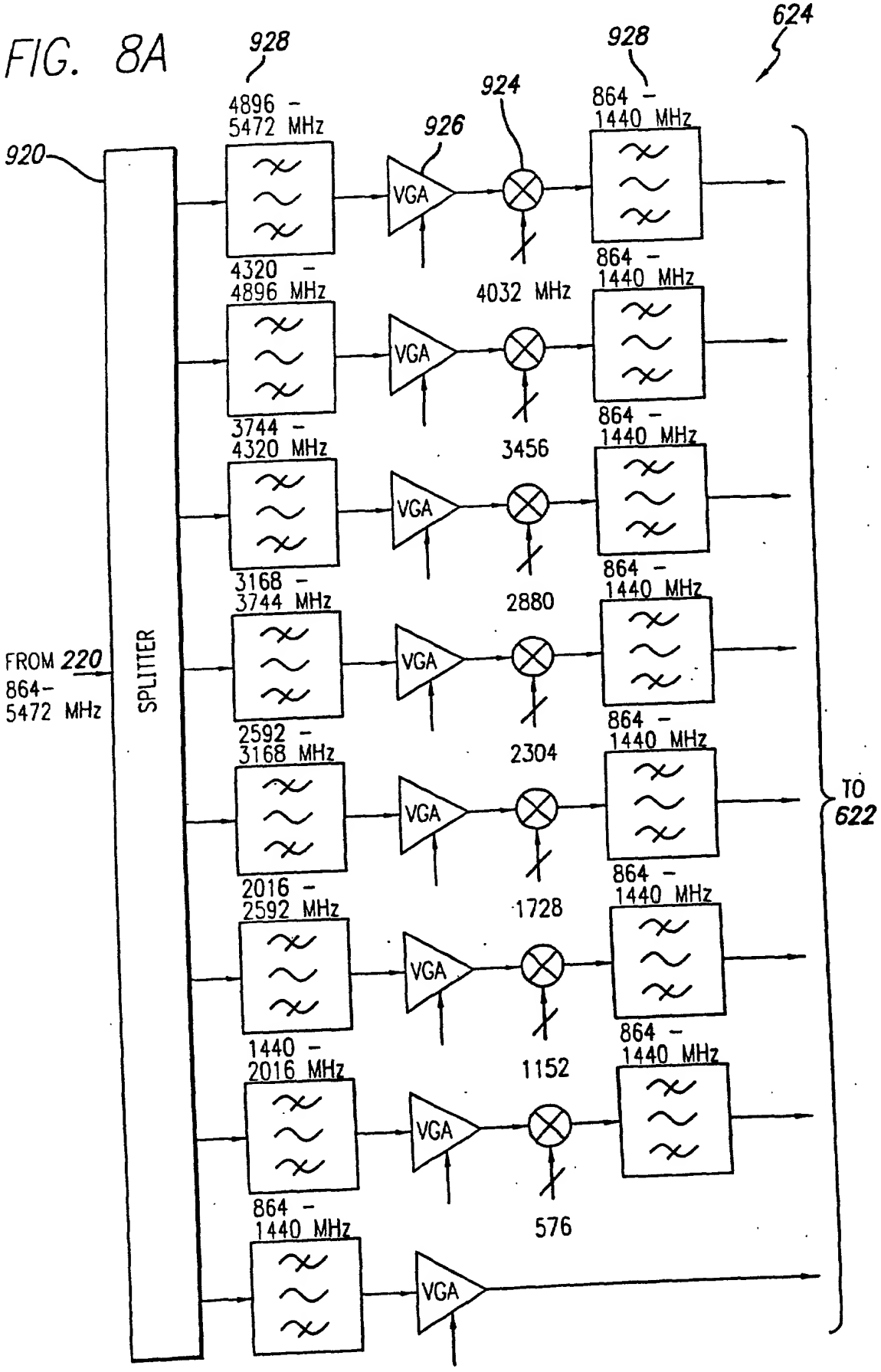
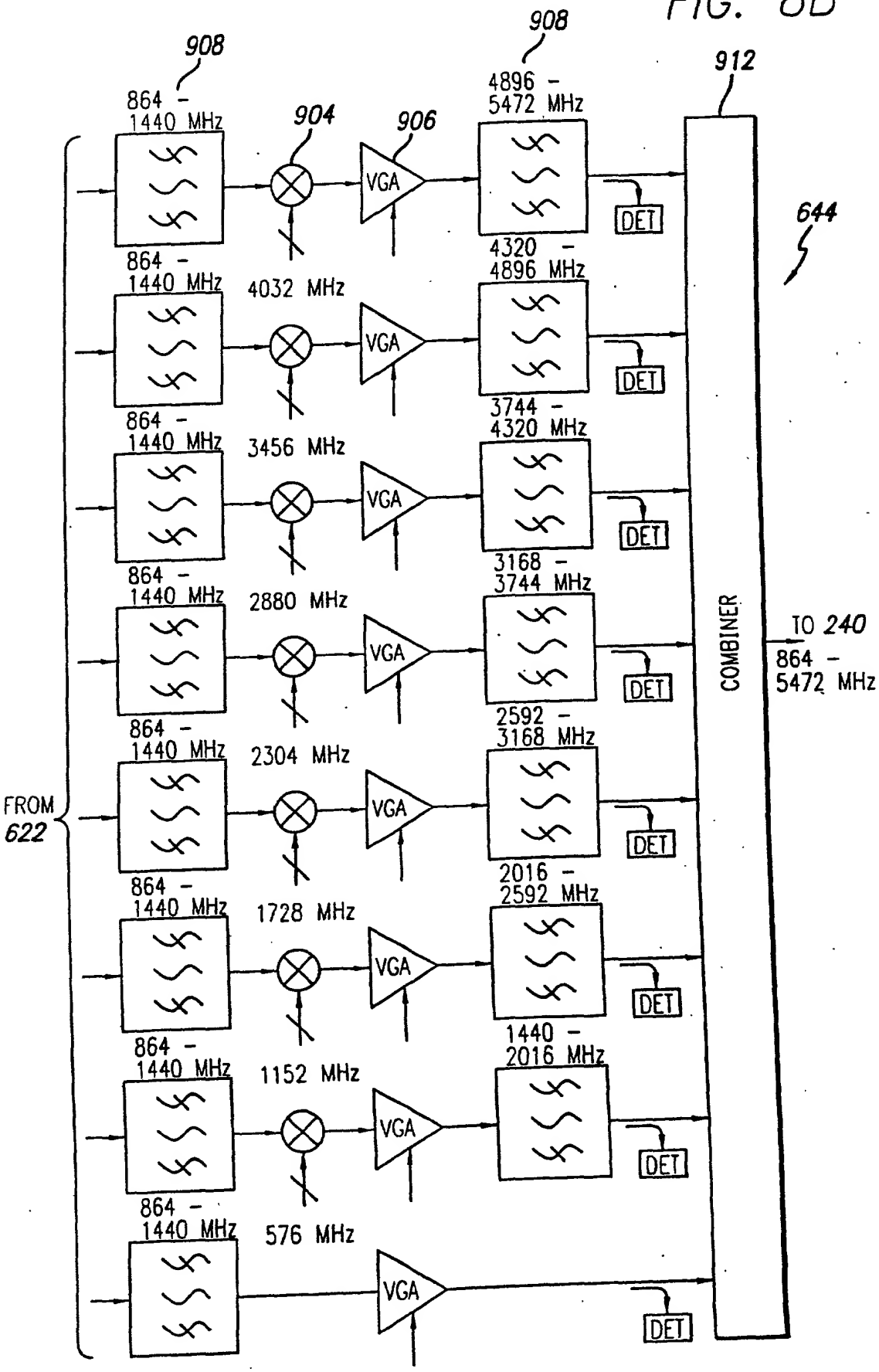
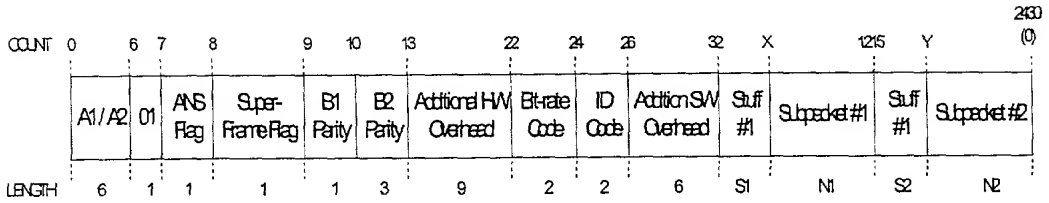

624
928
928
924
926
920
4896 - 5472 MHz
VGA
4032 MHz
864 - 1440 MHz
4320 - 4896 MHz
3744 - 4320 MHz
3456
3168 - 3744 MHz
2880
2592 - 3168 MHz
2304
2016 - 2592 MHz
1728
1440 - 2016 MHz
1152
864 - 1440 MHz
576
FROM 220
864 - 5472 MHz
SPLITTER
TO 622

FIG. 8B


908
908
912
904
906
644
FROM 622
TO 240
COMBINER
VGA
DET
864 - 1440 MHz
4896 - 5472 MHz
4320 - 4896 MHz
4032 MHz
3744 - 4320 MHz
3456 MHz
3168 - 3744 MHz
2880 MHz
2592 - 3168 MHz
2304 MHz
2016 - 2592 MHz
1728 MHz
1440 - 2016 MHz
1152 MHz
576 MHz



A1/A2 bytes - SONET header for STS3.

Additional S/W Overhead - 6 bytes

Additional H/W Overhead - 9 bytes

Subpacket - target bytes carried in frame. Two subpackets to reduce system latency.

Stuff - stuff bytes to fill unused parts of packet.

Parity - 1 byte parity for performance monitoring.

N1 - subpacket 1 byte count
N2 - subpacket 2 byte count
N1 + N2 = N (target signal bytes per frame)
S1 - Stuff #1 byte count
S2 - Stuff #2 byte count
X - Stuff #1 end count. Memory mapped register
Y - Stuff #2 end count. Memory Mapped register
T - Target Signal Data Rate

$N = T/(8\text{K-Hz}) * (1/8) * (1/4)$ bytes/frame

S1 + S2 = 2430 - N - 32 bytes/frame

Figure 9

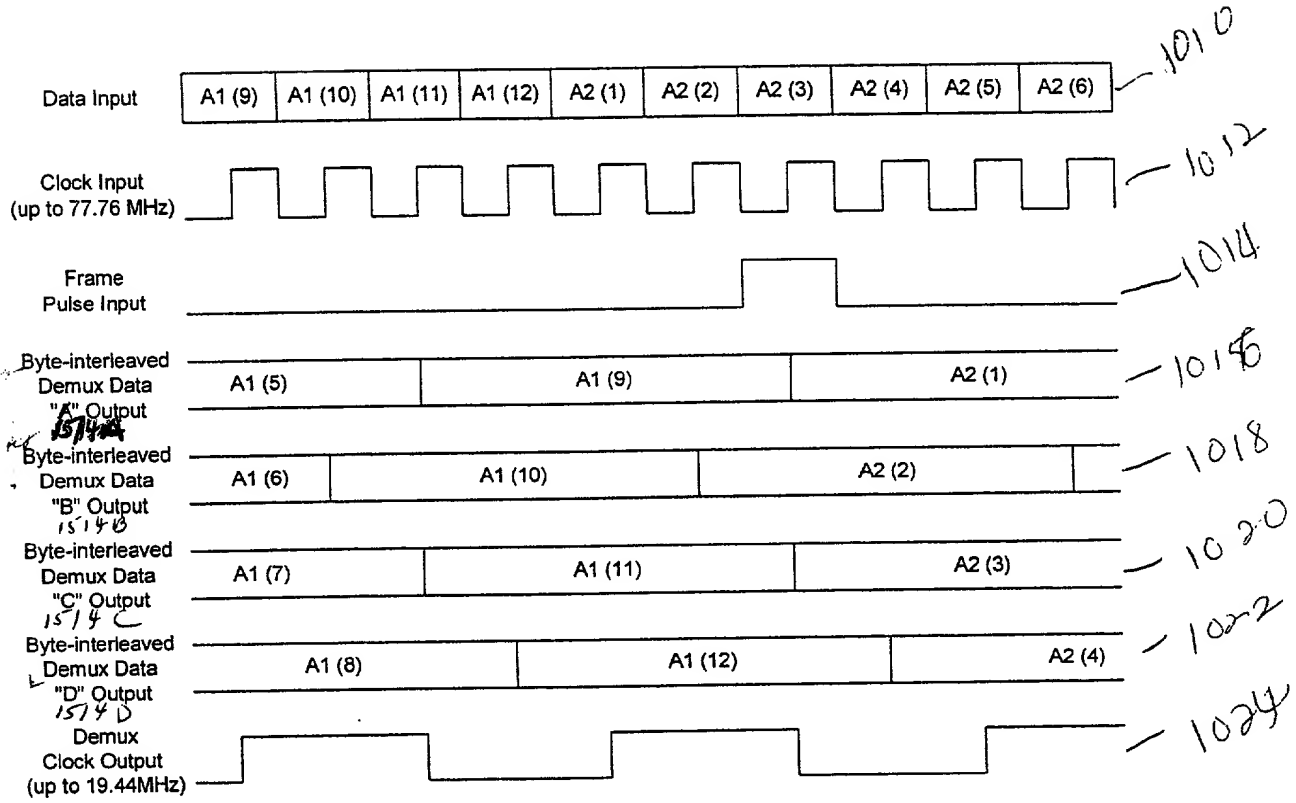

Data Input
A1 (9)
A1 (10)
A1 (11)
A1 (12)
A2 (1)
A2 (2)
A2 (3)
A2 (4)
A2 (5)
A2 (6)
1010
Clock Input
(up to 77.76 MHz)
1012
Frame
Pulse Input
1014
Byte-interleaved
Demux Data
"A" Output
1514A
A1 (5)
A1 (9)
A2 (1)
1016
Byte-interleaved
Demux Data
"B" Output
1514B
A1 (6)
A1 (10)
A2 (2)
1018
Byte-interleaved
Demux Data
"C" Output
1514C
A1 (7)
A1 (11)
A2 (3)
1020
Byte-interleaved
Demux Data
"D" Output
1514D
A1 (8)
A1 (12)
A2 (4)
1022
Demux
Clock Output
(up to 19.44MHz)
1024

Figure 10

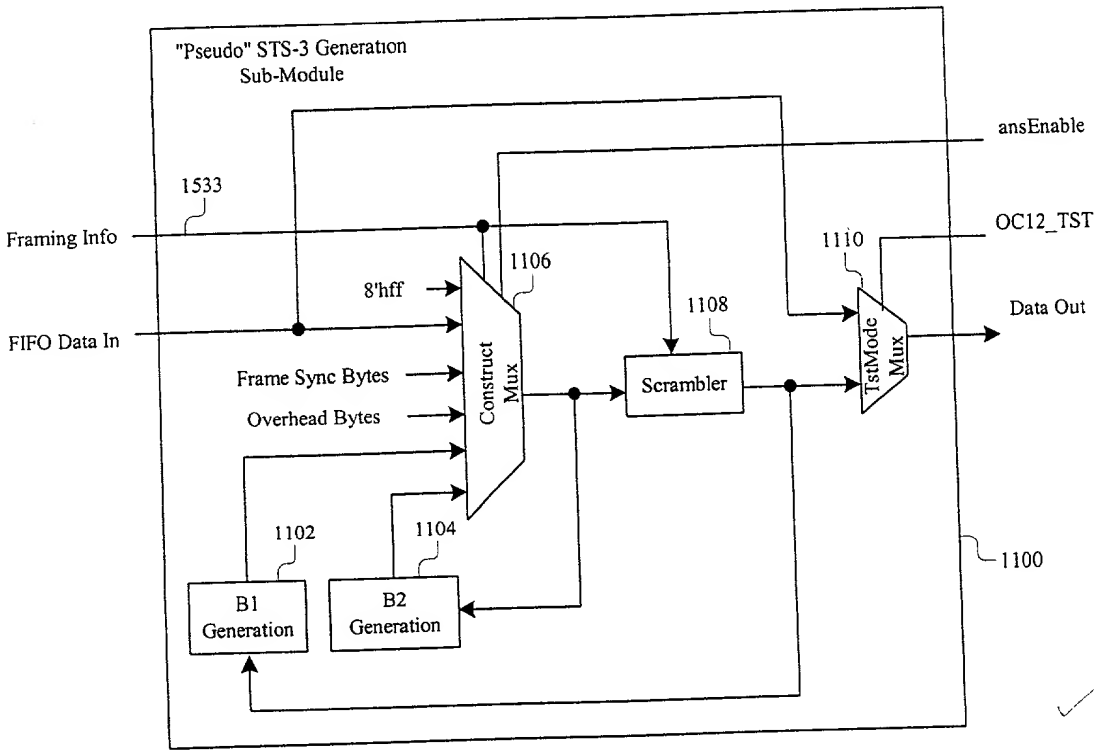

"Pseudo" STS-3 Generation
Sub-Module
ansEnable
1533
Framing Info
OC12_TST
1110
1106
8'hff
1108
Data Out
FIFO Data In
Construct Mux
TstMode Mux
Frame Sync Bytes
Scrambler
Overhead Bytes
1102
1104
1100
B1 Generation
B2 Generation

Figure 11

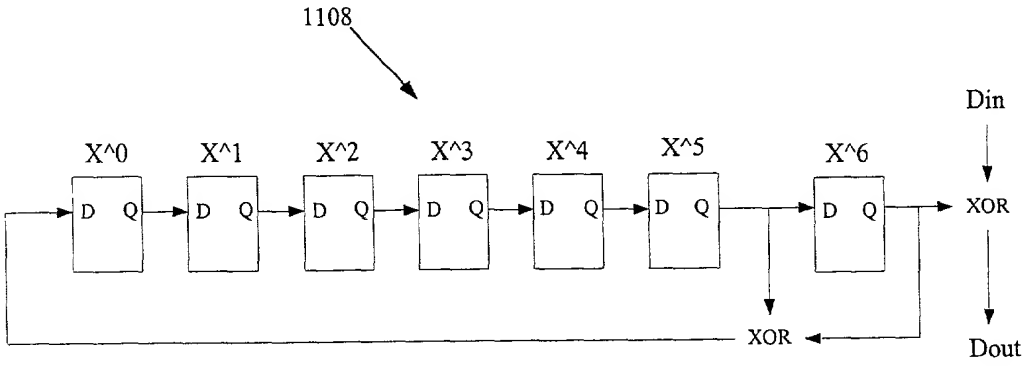


Figure 12

Docket No. 20852-05135

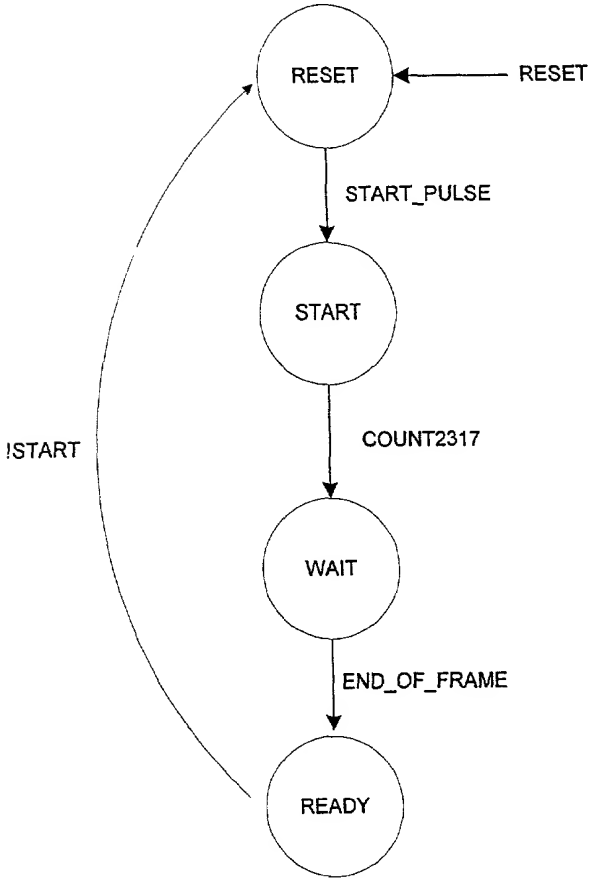

RESET
RESET
START_PULSE
START
COUNT2317
!START
WAIT
END_OF_FRAME
READY

Figure 13

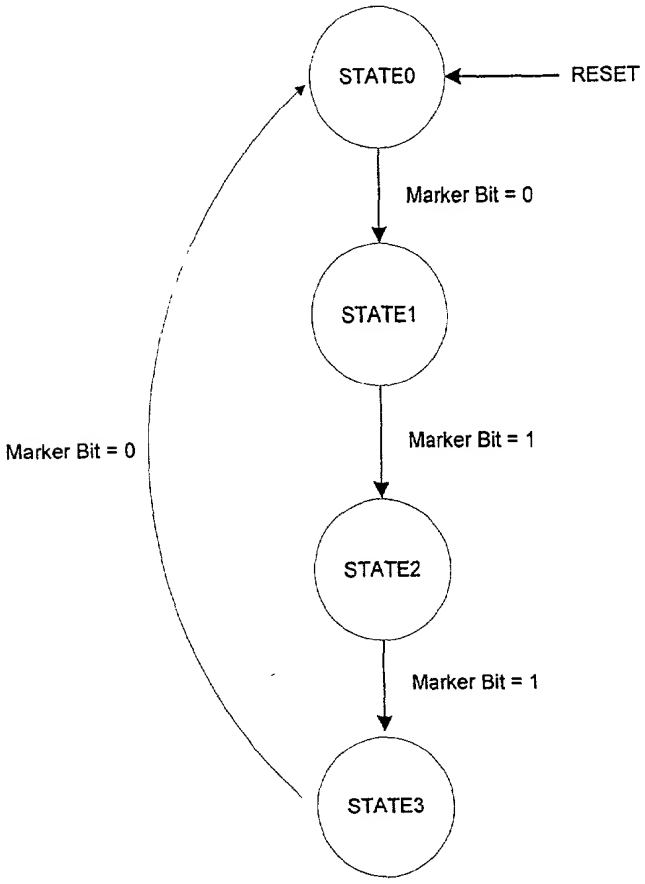

STATE0
RESET
Marker Bit = 0
STATE1
Marker Bit = 1
Marker Bit = 0
STATE2
Marker Bit = 1
STATE3

Figure 14

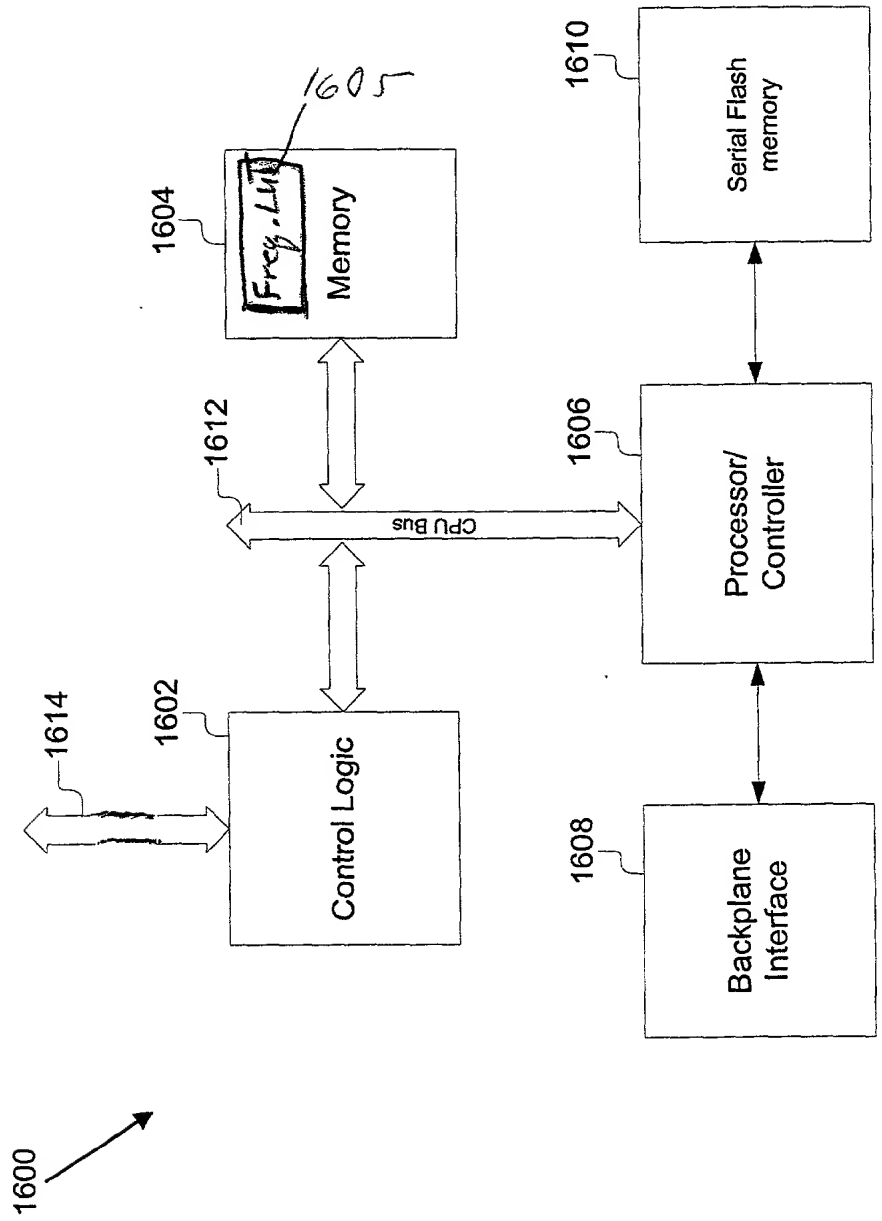

1600
1602
Control Logic
1604
Memory
1605
Freq. Lut
1606
Processor/
Controller
1608
Backplane
Interface
1610
Serial Flash
memory
1612
CPU Bus
1614

Figure 15

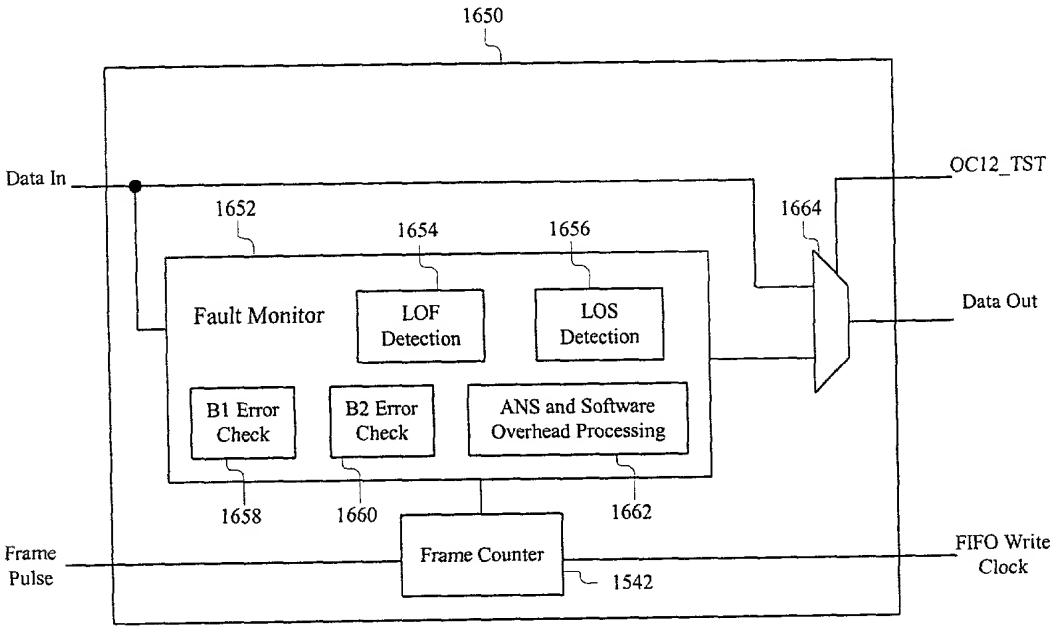

1650
Data In
OC12_TST
1652
1654
1656
1664
Fault Monitor
LOF Detection
LOS Detection
Data Out
B1 Error Check
B2 Error Check
ANS and Software Overhead Processing
1658
1660
1662
Frame Pulse
Frame Counter
FIFO Write Clock
1542

Figure 16

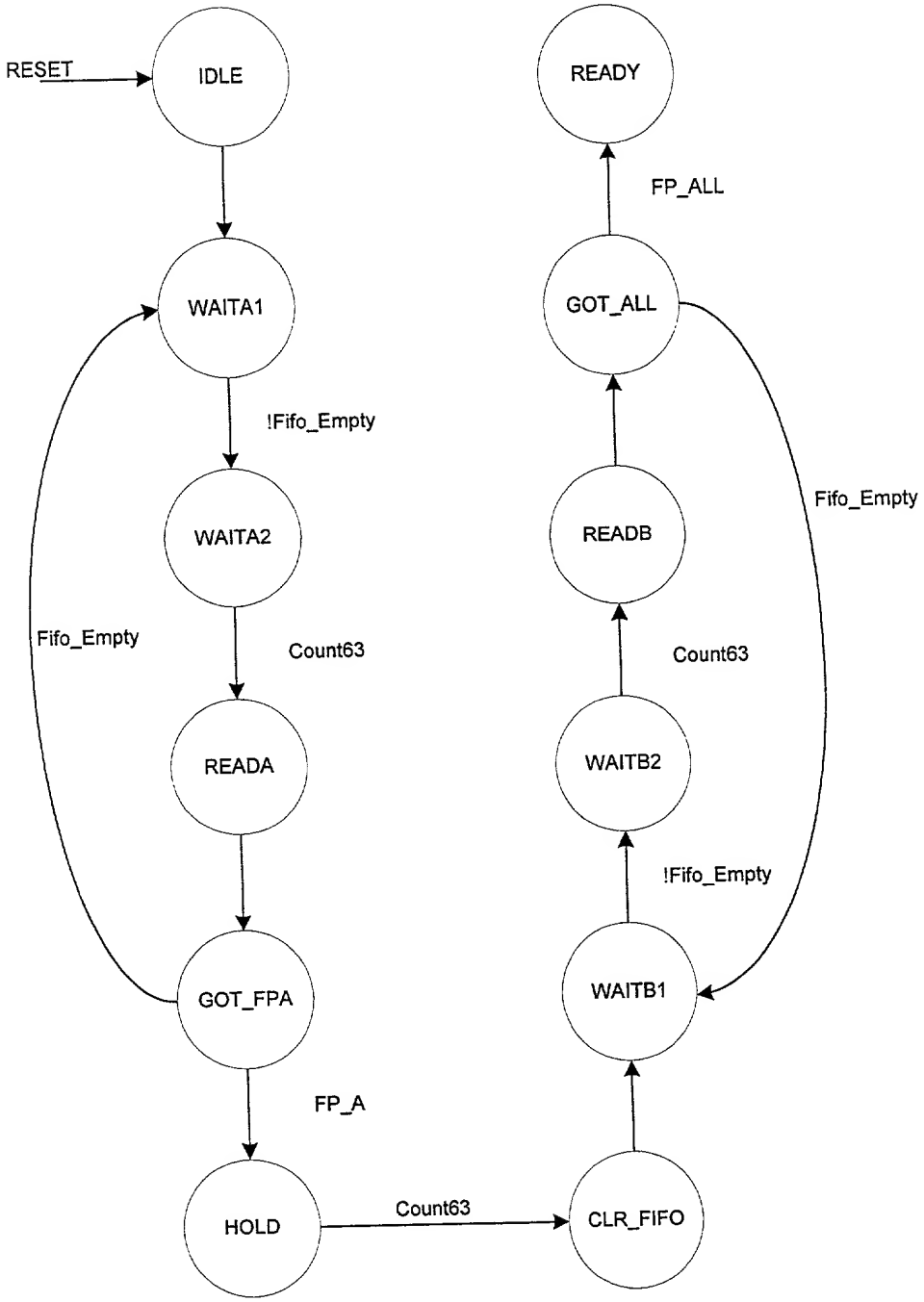

RESET
IDLE
WAITA1
!Fifo_Empty
WAITA2
Fifo_Empty
Count63
READA
GOT_FPA
FP_A
HOLD
Count63
CLR_FIFO
WAITB1
!Fifo_Empty
WAITB2
Count63
READB
Fifo_Empty
GOT_ALL
FP_ALL
READY

Figure 17

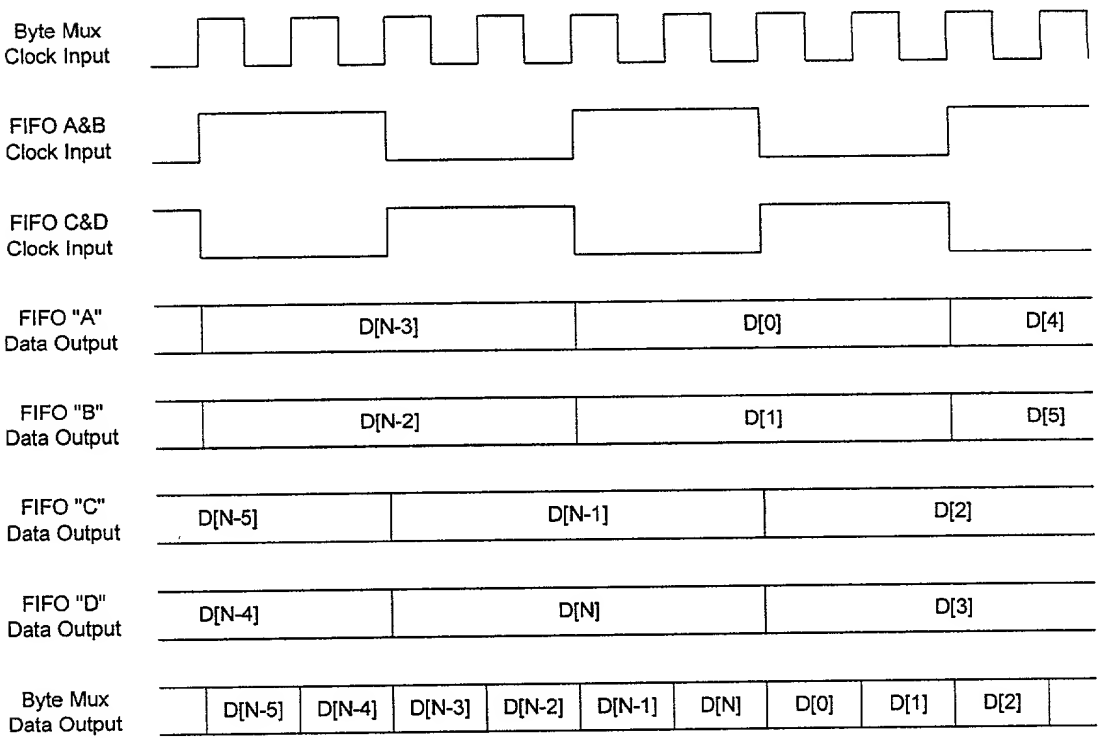

Byte Mux Clock Input
FIFO A&B Clock Input
FIFO C&D Clock Input
FIFO "A" Data Output
D[N-3]
D[0]
D[4]
FIFO "B" Data Output
D[N-2]
D[1]
D[5]
FIFO "C" Data Output
D[N-5]
D[N-1]
D[2]
FIFO "D" Data Output
D[N-4]
D[N]
D[3]
Byte Mux Data Output
D[N-5]
D[N-4]
D[N-3]
D[N-2]
D[N-1]
D[N]
D[0]
D[1]
D[2]

Figure 18